CLAIMS

Claims 1-22 *(CANCELLED)*

23. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said

one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

24. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

25. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

26. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said

control circuitry to said one or more local control signals.

27. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

28. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

29. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

30. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

31. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein: said first pipeline subcircuitry portion is further responsive to said active

first clock signal by performing at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction; and

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states.

32. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

33. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

34. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said control circuitry comprises logic circuitry that converts said one or more local control signals to said one or more clock control signals.

35. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

36. *(PREVIOUSLY PRESENTED)* The apparatus of claim 23, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

37. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions;

controller means for responding to said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power

management instruction; and

clock source means for responding to said one or more clock control signals by generating at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

38. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said one or more local control signals by providing one or more clock control

signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

39. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

40. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

41. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first

clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

42. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

43. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

44. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

45. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

46. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein:

said first pipeline subcircuitry portion is further responsive to said active first clock signal by performing at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction;

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states; and

said clock circuitry is further responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

47. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

48. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more clock control signals.

49. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said control circuitry comprises logic circuitry that converts said one or more local

control signals to said one or more clock control signals.

50. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

51. *(PREVIOUSLY PRESENTED)* The apparatus of claim 38, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

52. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions;

controller means for responding to said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock source means for responding to said one or more clock control signals by generating at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

53. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and

de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

54. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

55. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having

respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

56. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

57. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

58. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

59. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a

plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

60. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

61. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein:

said first pipeline subcircuitry portion is further responsive to said active first clock signal by performing at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction; and

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states.

62. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

63. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

64. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said control circuitry comprises logic circuitry that converts said one or more local control signals to said one or more clock control signals.

65. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

66. *(PREVIOUSLY PRESENTED)* The apparatus of claim 53, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

67. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective

assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions;

controller means for responding to said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock source means for responding to said one or more clock control signals by generating at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

68. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to at least a

first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

69. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded

instructions prior to said response by said control circuitry to said one or more local control signals.

70. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

71. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

72. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

73. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said

execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

74. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

75. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

76. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein:

said first pipeline subcircuitry portion is further responsive to said active first clock signal by performing at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction;

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states; and

said clock circuitry is further responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal

active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

77. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

78. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more clock control signals.

79. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said control circuitry comprises logic circuitry that converts said one or more local control signals to said one or more clock control signals.

80. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

81. *(PREVIOUSLY PRESENTED)* The apparatus of claim 68, wherein said clock circuitry further provides a second clock signal with active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

82. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to at least a first one of said plurality of first clock signal cycles by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to at least a second one subsequent to said first one of said plurality of first clock signal cycles by executing said one or more decoded instructions;

controller means for responding to said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock source means for responding to said one or more clock control signals by generating at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

83. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said first clock signal, a second clock signal and said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock circuitry coupled to said control circuitry and said plurality of subcircuits, and responsive to said one or more clock control signals by providing

said first and second clock signals with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.

84. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

85. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

86. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

87. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein

said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

88. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

89. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

90. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

91. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein:

said first pipeline subcircuitry portion is further responsive to said active first clock signal by performing at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming

instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction; and

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states.

92. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

93. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

94. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said control circuitry comprises logic circuitry that converts said one or more local control signals to said one or more clock control signals.

95. *(PREVIOUSLY PRESENTED)* The apparatus of claim 83, wherein said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

96. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions,

including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions;

controller means for responding to said first clock signal, a second clock signal and said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

clock source means for responding to said one or more clock control signals by generating said first and second clock signals with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.

97. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

a plurality of interface electrodes to convey at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

a plurality of subcircuits coupled to at least a portion of said plurality of interface electrodes and including pipeline subcircuitry responsive to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline subcircuitry is responsive to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline subcircuitry is coupled to said first pipeline subcircuitry portion and responsive to said active first clock signal by executing said one or more decoded instructions;

control circuitry coupled to said plurality of subcircuits and responsive to said first clock signal, a second clock signal and said one or more local control signals by providing one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock circuitry coupled to said control circuitry and said plurality of

subcircuits, and responsive to said one or more clock control signals by providing said first and second clock signals with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction, and with said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.

98. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

99. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

100. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

101. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a deactivation of said first clock signal by retaining, until a reactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

102. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said control circuitry to said one or more local control signals.

103. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said plurality of subcircuits further includes data storage circuitry responsive to a reactivation following a deactivation of said first clock signal by providing a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said response by said clock circuitry to said one or more clock control signals.

104. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said first pipeline subcircuitry portion comprises decoding circuitry.

105. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein:

said first pipeline subcircuitry portion is further responsive to said active first clock signal by performing at least another one or more respective portions of

said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions to provide said one or more local control signals with another one or more respective assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction;

said control circuitry is further responsive to said another one or more respective assertion and de-assertion states of said one or more local control signals by providing said one or more clock control signals with another one or more respective assertion and de-assertion states; and

said clock circuitry is further responsive to said one or more clock control signals by providing at least said first clock signal with said first clock signal active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

106. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said second pipeline subcircuitry portion comprises arithmetic logic circuitry.

107. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said control circuitry further provides a status signal indicative of said one or more respective assertion and de-assertion states of said one or more clock control signals.

108. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein said control circuitry comprises logic circuitry that converts said one or more local control signals to said one or more clock control signals.

109. *(PREVIOUSLY PRESENTED)* The apparatus of claim 97, wherein

said control circuitry comprises at least one register in which said one or more local control signals are stored to provide said one or more clock control signals.

110. *(PREVIOUSLY PRESENTED)* An apparatus including integrated processor circuitry, said apparatus comprising:

interface means for conveying at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

subcircuit means including pipeline means for responding to a first clock signal having active and inactive states by selectively operating on one or more of said plurality of incoming instructions for data processing, wherein

a first portion of said pipeline means is for responding to said active first clock signal by performing at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions to provide one or more decoded instructions and to provide one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction, and

a second portion of said pipeline means is for responding to said active first clock signal by executing said one or more decoded instructions;

controller means for responding to said first clock signal, a second clock signal and said one or more local control signals by generating one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

clock source means for responding to said one or more clock control signals by generating said first and second clock signals with said first clock signal

inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction, and with said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.